Appl. No. 10/733,626
Examiner: Nhu, David, Art Unit 2818
In response to the Office Action dated April 4, 2005

Date: July 3, 2005
Attorney Docket No. 10113421

REMARKS

Responsive to the Office Action mailed on April 4, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-13 are withdrawn from consideration. Claims 14, 20 and 21 are objected to for informalities. Claims 14-37 are rejected under the judicially created doctrine of obviousness-type double patenting over claims 12-30 of U.S. Patent No. 6,818,948. Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al (U.S. Patent No. 6,093,606).

In this paper, claims 14 and 21 are amended to overcome the objections as described in further detail below. Withdrawn claims 1-13 are canceled in favor of a divisional application filed thereto. Thus, on entry of this amendment, claims 14-37 are pending.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Objections to the Claims

Claims 14, 20 and 21 are objected to for informalities. In this paper, claim 14 is amended according to the suggestion of the Examiner. Claim 21 is amended to depend from claim 20. As claim 14 provides antecedent basis for "the bottom" of each long trench, and claims 20 and 21 depend either directly or indirectly from claim 14, it is Applicant's belief that the objections to claims 14, 20 and 21 are thereby overcome.

Double Patenting Rejections

Claims 14-37 are rejected under the judicially created doctrine of obviousness-type double patenting over claims 12-30 of U.S. Patent No. 6,818,948. Applicant respectfully traverses the rejections for the reasons as follow.

Claim 14, recites a method of fabricating stacked gate flash memory cells, comprising the steps of:

> ... forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby;
>
> forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer;
>
> forming a pair of inter-gate dielectric layers, respectively overlying the floating gate;
>
> forming a pair of control gates, respectively overlying the inter-gate dielectric layer ...

Thus, claim 14 recites a method for fabricating a ***dual bit*** stacked gate flash memory device, since a pair of floating gates are formed on the source isolation layer, a pair of inter-gate dielectric layers are formed overlying the floating gates and a pair of control gates are formed overlying the inter-gate dielectric layers. In contrast, claims 12-30 of U.S. Patent No. 6,818,948 disclose a method for fabricating a ***single bit*** stacked gate flash memory device since there is only a single control gate and a single floating gate formed in each cell trench.

Furthermore, in the method of claim 14, the control gates and floating gates are formed ***along the sidewalls of the trench***. This provides a larger overlapping area than that of the method recited in claims 12-30 of U.S. Patent No. 6,818,948 B2, in which the single control gate and floating gate are horizontally stacked in the cell trench. The larger overlapping area provided by the method recited in claim 14 allows for a higher coupling ratio than that achievable by the method recited in claims 12-30 of U.S. Patent No. 6,818,948.

Applicant therefore submits that the differences between the invention recited in claims 14-37 of the present application and claims 12-30 of U.S. Patent No. 6,818,948 are significant, and that a person of ordinary skill in the art would not conclude that the invention defined in claims 14-37 of the present application is an obvious variation of the invention defined in claims 12-30 of U.S. Patent No. 6,818,948. Withdrawal of the double patenting rejection of claims 12-30 is respectfully requested.

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Rejections Under 35 U.S.C. 102(b)

Claim 14 is rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. The rejection is respectfully traversed for the reasons as follow.

To anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
>
> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 14, recites a method of fabricating stacked gate flash memory cells, comprising the steps of:

> ... forming a conductive layer and ***a pair of source regions on a bottom of each long trench***, ***wherein the source regions are*** respectively disposed in the substrate adjacent to two sidewalls of each long trench and ***electrically connected to the conductive layer***;
>
> forming a source isolation layer on each conductive layer;
>
> forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby;
>
> forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer;
>
> forming a pair of inter-gate dielectric layers, respectively overlying the floating gate;
>
> ***forming a pair of control gates***, respectively overlying the inter-gate dielectric layer;

forming an insulating layer in each long trench, isolating the control gates

...

In contrast, in Lin et al, an oxide layer 22 is formed between a source (S) and a conductive layer (PS1). See Figs. 1H and 2H of Lin et al. Thus, it is impossible for the source to be ***electrically connected*** to the conductive layer, as recited in claim 14.

Furthermore, in Lin et al, only a single control gate (CG) and a single source (S) are formed in each cell. See Figs. 1K and 2K of Lin et al. Thus, Lin et al fail to teach the steps of forming a ***pair*** of source regions and forming a ***pair*** of control gates in each cell, as recited in claim 14.

Furthermore, the insulating film 34 disclosed in Lin et al is formed above the trench. See Fig. 1L of Lin et al. Thus, Lin et al fail to teach the step of forming an insulating layer ***in*** each long trench, as recited in claim 14.

For at least the reasons described above, it is Applicant's belief that Line et al fails to teach or suggest all the limitations of claim 14. Applicant therefore respectfully requests that rejection of claim 14 be withdrawn and the claim passed to issue. Insofar as claims 15-37 depend from claims 14 either directly or indirectly, and therefore incorporate all of the limitations of claim 14, it is Applicant's belief that these claims are also in condition for allowance.

Foreign Priority Claim

Acknowledgment of Applicant's claim to foreign priority under 35 USC 119(a)-(d) or (f) and receipt of the certified copies of the priority document(s) is respectfully requested. In this regard, Applicant notes that box 12(a)(1) of the Office Action Summary is not checked.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

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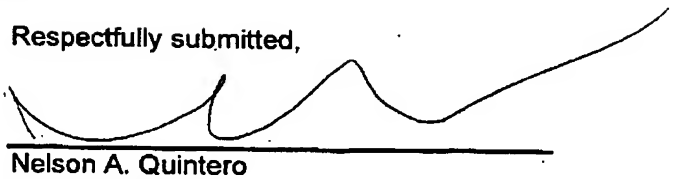
Respectfully submitted,



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